RECTRON SEMICONDUCTOR
TECHNICAL SPECIFICATION

RM50N60DFV

N-Channel Enhancement Mode Power MOSFET

Description

The RM50N60DFV uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

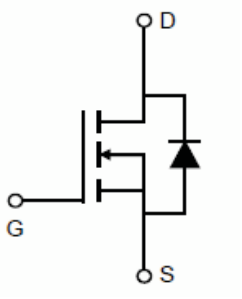
General Features

- V_{DS} =60V,I_D =50A
  $R_{DS(ON)}$ < 16mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ < 20mΩ @ V_{GS}=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

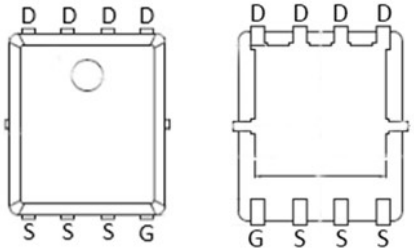
Application

- PWM
- Load Switching
- P/N suffix V means AEC-Q101 qualified, e.g:RM50N60DFV
- Halogen-free

100% UIS TESTED!
100% ΔVds TESTED!



Schematic Diagram



Top View **Bottom View**

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
50N60	RM50N60DFV	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (T_a =25℃)	I_D	50	A
Continuous Drain Current (T_a =100℃)	I_D	33	A
Pulsed Drain Current (1)	I_{DM}	160	A
Single Pulsed Avalanche Energy (2)	E_{AS}	64	mJ
Power Dissipation	P_D	54	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.74	℃/W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	50	℃/W
Junction Temperature	T_J	175	℃
Storage Temperature	T_{STG}	-55~ +175	℃

Electrical Characteristics (T_C=25℃unless otherwise noted)

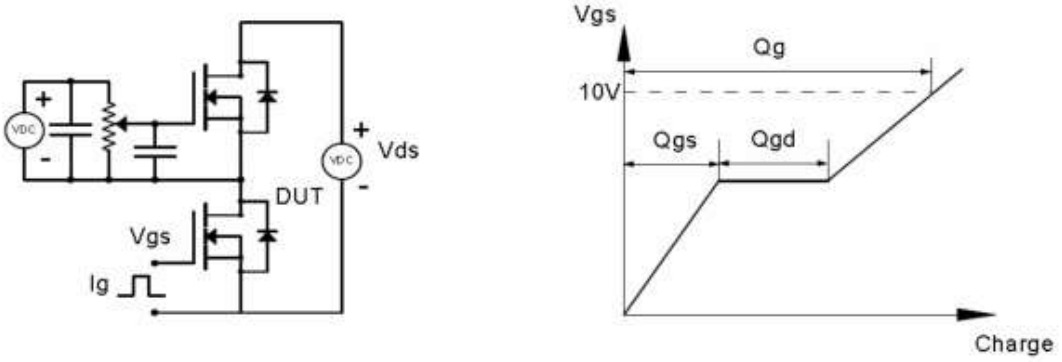
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	60	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} =60V, V_{GS} = 0V	-	-	1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V	-	-	±100	nA
Gate threshold voltage(3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1	1.6	2.2	V
Drain-source on-resistance(3)	$R_{DS(on)}$	V_{GS} =10V, I_D =20A	-	13.2	16	mΩ
		V_{GS} =4.5V, I_D =15A	-	15.2	20	
Forward tranconductance(3)	g_{FS}	V_{DS} =5V, I_D =10A	20	-	-	S
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =25V, V_{GS} =0V, f =1MHz	-	2600	-	pF
Output Capacitance	C_{oss}		-	125	-	
Reverse Transfer Capacitance	C_{rss}		-	105	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=30V, I_D=20A V_{GS}=10V, R_G=1.8Ω	-	4	-	ns
Turn-on rise time	t_r		-	8	-	
Turn-off delay time	$t_{d(off)}$		-	27	-	
Turn-off fall time	t_f		-	20	-	
Total Gate Charge	Qg	VDS=30V, ID=20A, VGS=10V	-	51	-	nC
Gate-Source Charge	Qgs		-	7.9	-	
Gate-Drain Charge	Qgd		-	8.1	-	
Source-Drain Diode characteristics						
Diode Forward voltage(3)	V_{SD}	V_{GS} =0V, I_S=20A	-	-	1.2	V
Diode Forward current(4)	I_S		-	-	50	A
Body Diode Reverse Recovery Time	trr	T_J=25°， IF=20A,di/dt=100A/us		21		ns
Body Diode Reverse Recovery Charge	Qrr	T_J=25°， IF=20A,di/dt=100A/us		18		nc

Notes:

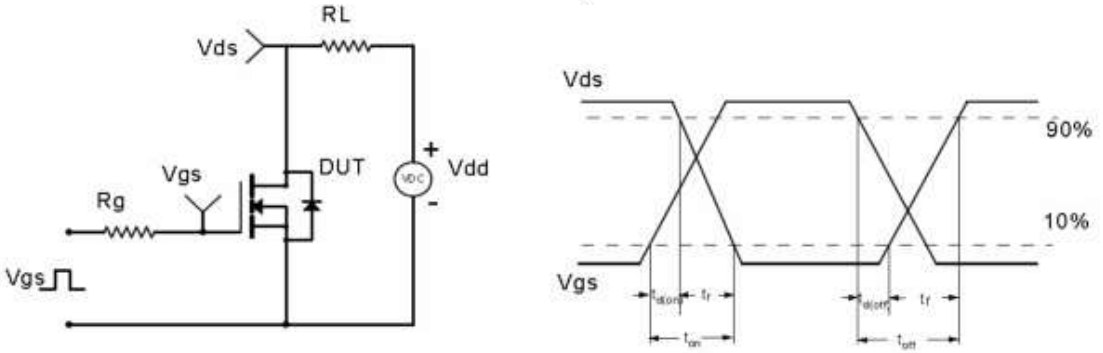
1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition:T_J=25℃,V_{DD}=30V,R_G=25Ω,L=0.5mH
3. Pulse Test: pulse width≤300μs, duty cycle≤0.5%
4. Surface Mounted on FR4 Board,t≤10 sec

Test Circuit & Waveform

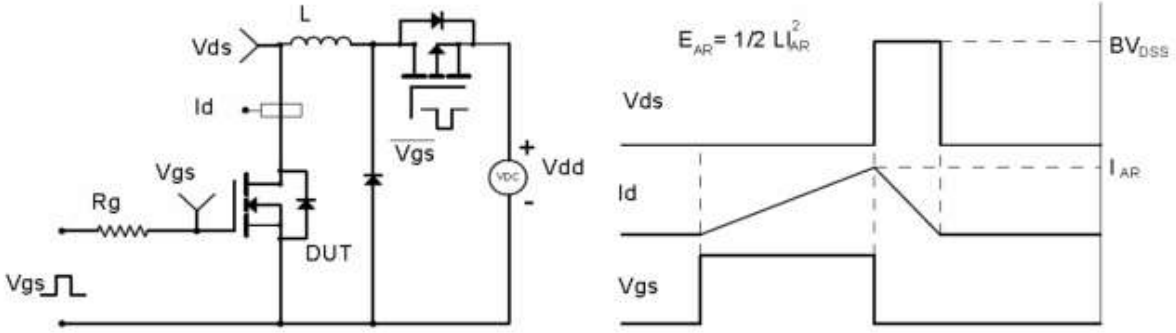
Gate Charge Test Circuit & Waveform



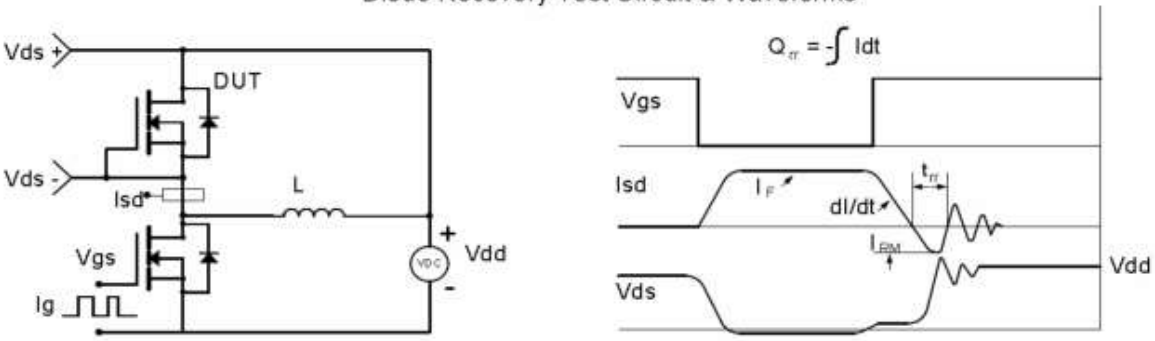
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



RATING AND CHARACTERISTICS CURVES (RM50N60DFV)

Figure1: Output Characteristics

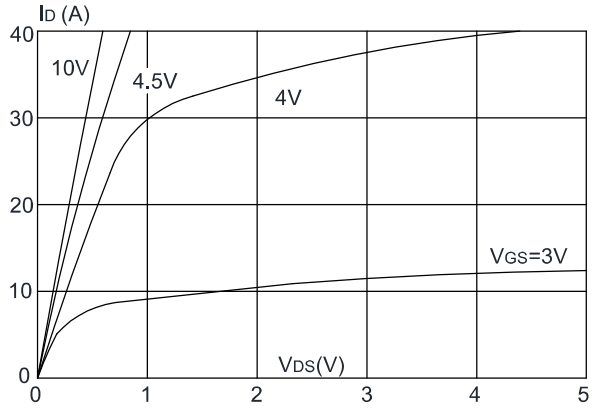


Figure 2: Typical Transfer Characteristics

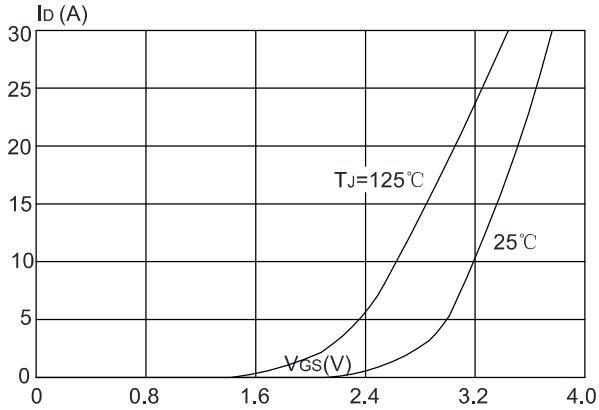


Figure 3: On-resistance vs. Drain Current

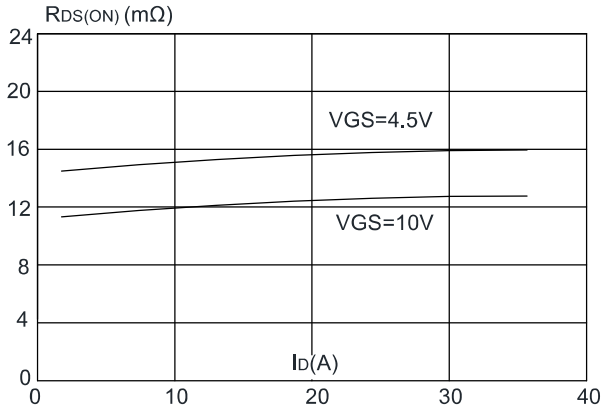


Figure 4: Body Diode Characteristics

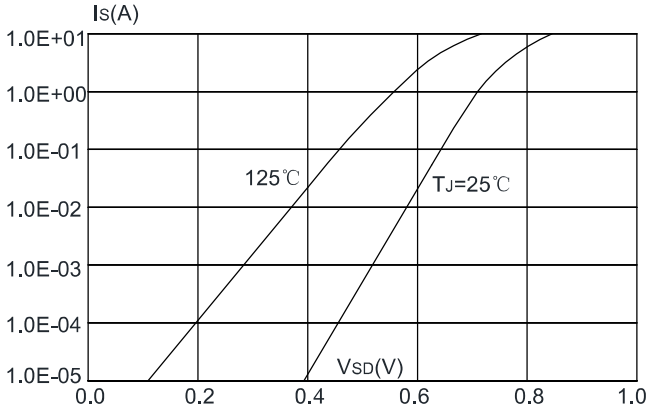


Figure 5: Gate Charge Characteristics

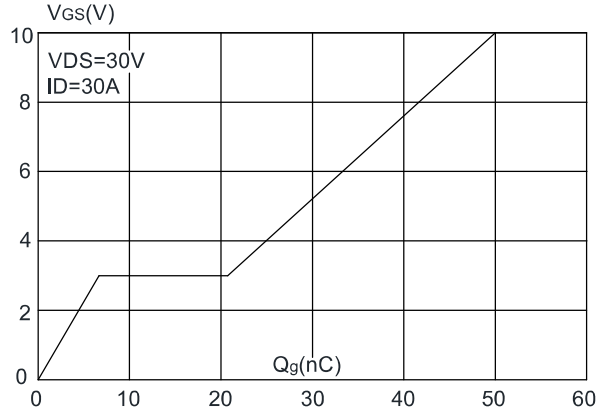
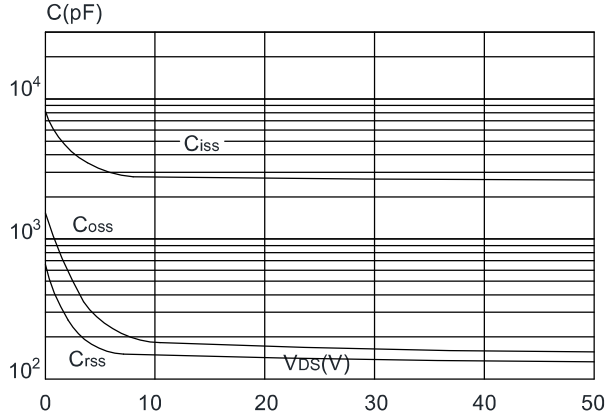


Figure 6: Capacitance Characteristics



RATING AND CHARACTERISTICS CURVES (RM50N60DFV)

Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

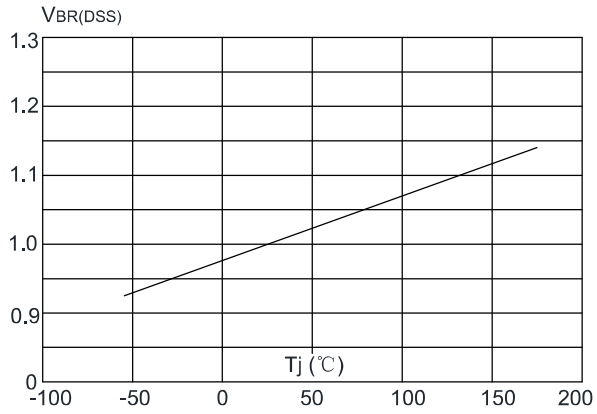


Figure 8: Normalized on Resistance vs. Junction Temperature

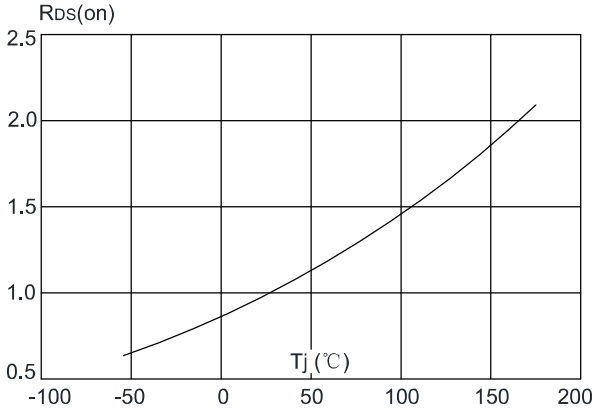


Figure 9: Maximum Safe Operating Area

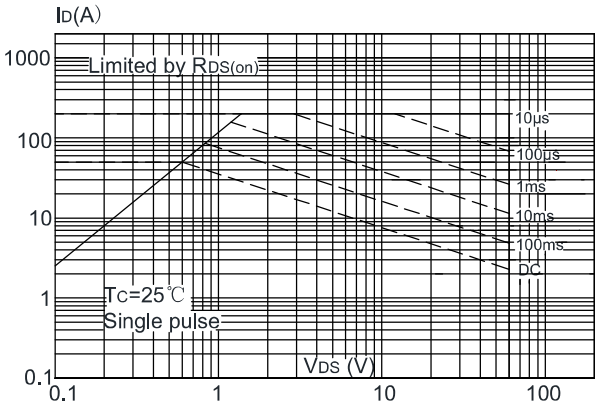


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

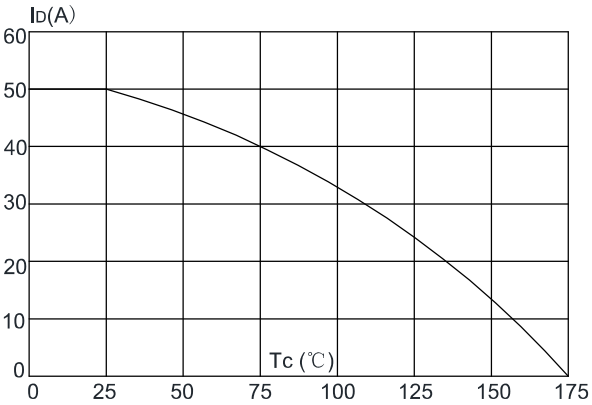
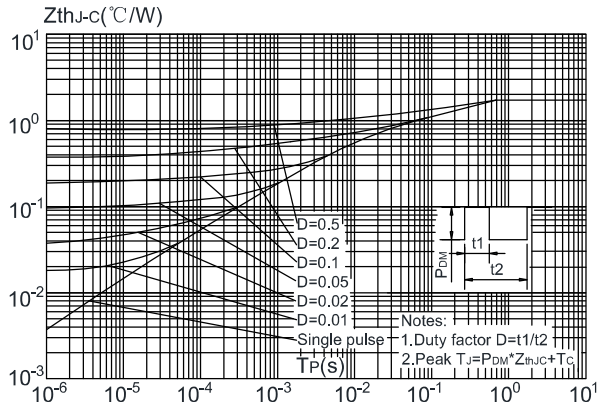
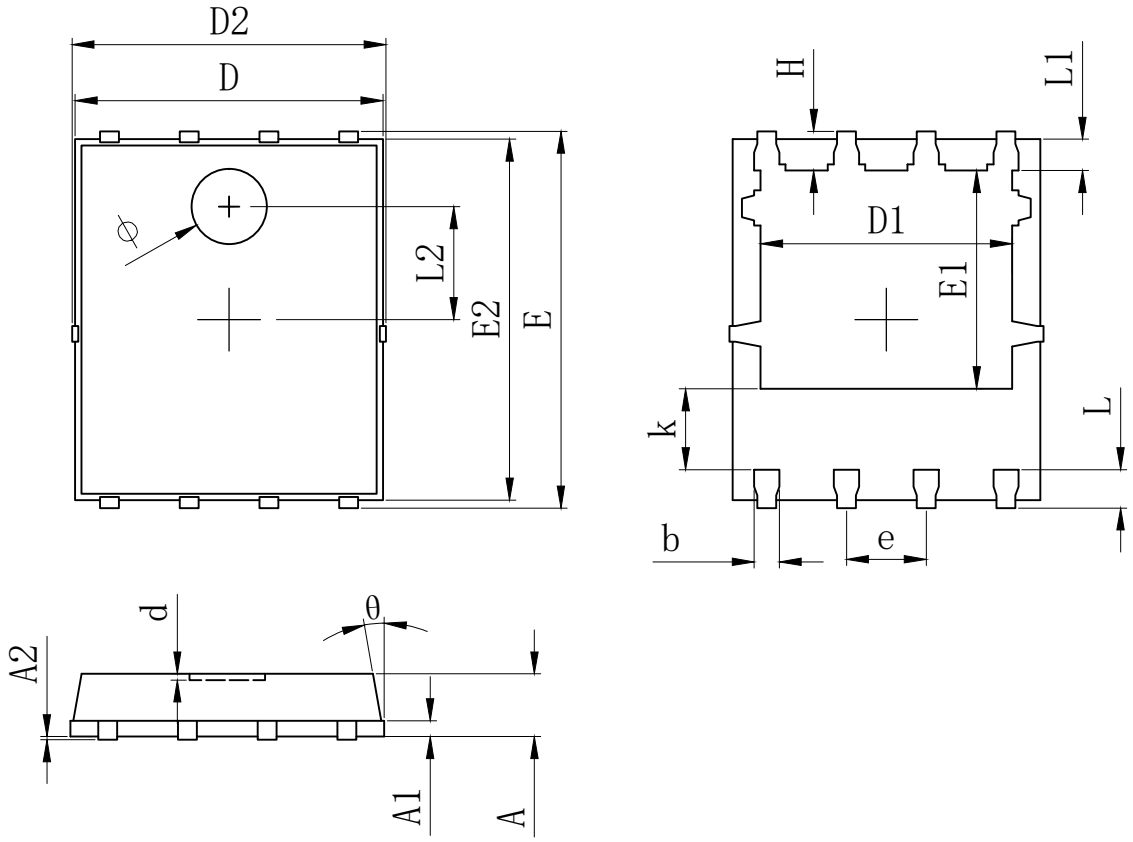


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



DFN5X6-8L Package Information



SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	0.900	1.000	1.100
A1	0.254 REF.		
A2	0~0.05		
D	4.824	4.900	4.976
D1	3.910	4.010	4.110
D2	4.924	5.000	5.076
E	5.924	6.000	6.076
E1	3.375	3.475	3.575
E2	5.674	5.750	5.826
b	0.350	0.400	0.450
e	1.270 TYP.		
L	0.534	0.610	0.686
L1	0.424	0.500	0.576
L2	1.800 REF.		
k	1.190	1.290	1.390
H	0.549	0.625	0.701
θ	8°	10°	12°
Φ	1.100	1.200	1.300
d			0.100

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