



# N-Channel SiC Power MOSFET G2 MOSFET Technology

#### **Features**

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitance
- Easy to Parallel and Simple to Drive
- P/N suffix V means AEC-Q101qualified, e.g:RSM33N1200D7LV

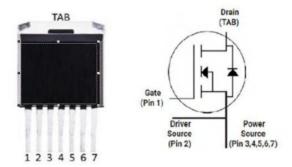
#### **Benefits**

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

#### **Applications**

- Renewable Energy
- EV Battery Chargers
- High Voltage DC/DC Converters
- Switch Mode Power Supplies
- Halogen-free

# $\begin{array}{cccccc} V_{DS} & = & 1200 & V \\ \\ R_{DS(on)} & = & 75 & m\Omega \\ \\ I_D@25^{\circ}C & = & 33 & A \end{array}$



#### **Package Marking and Ordering Information**

Device Marking Device		Device Package	Packaging Code	Reel Size	Quantity(PCS)	
33N120	RSM33N120D7LV	TO-263-7	-W	13inch	400	

#### Maximum Ratings (T<sub>c</sub>=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
$V_{DSmax}$	Drain-Source Voltage	1200	٧	V <sub>GS</sub> =0V, I <sub>D</sub> =100μA	
V <sub>GSmax</sub>	Gate-Source Voltage	-8/+22	٧	Absolute maximum values	
V <sub>GSop</sub>	Gate-Source Voltage	-4/+18	V	Recommended operational values	
	Continuous Drain Current	33		V <sub>GS</sub> =18V, T <sub>c</sub> =25°C	Fig. 19
I <sub>D</sub>		23.8	A	V <sub>GS</sub> =18V, T <sub>c</sub> =100°C	
I <sub>D(pulse)</sub>	Pulsed Drain Current	80	Α	Pulse width t <sub>p</sub> limited by T <sub>Jmax</sub>	Fig. 22
P <sub>D</sub>	Power Dissipation	136	w	T <sub>c</sub> =25°C, T <sub>J</sub> =175°C	Fig. 20
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature	-55 to +175	°C		
TL	Solder Temperature, 1.6mm from case for 10s	260	°C		
	Mounting Torque, (M3 or 6-32 screw)	1	Nm		
$M_d$		8.8	lbf-in		

# Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions	Note	
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	1200	/	/	V	V <sub>GS</sub> =0V, I <sub>D</sub> =100μA		
	0.71	1.9	2.6	4.0	.,	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =5mA	F:- 44	
$V_{GS(th)}$	Gate Threshold Voltage	/	1.8	/	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =5mA, T <sub>J</sub> =175°C	Fig. 11	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	/	1	100	μΑ	V <sub>DS</sub> =1200V, V <sub>GS</sub> =0V		
I <sub>GSS+</sub>	Gate-Source Leakage Current	/	10	250	nA	V <sub>DS</sub> =0V, V <sub>GS</sub> =22V		
I <sub>GSS-</sub>	Gate-Source Leakage Current	/	10	250	nA	V <sub>DS</sub> = <b>0</b> V, V <sub>GS</sub> =- <b>8</b> V		
В	Drain Source On State Besistance	/	75	95	mΩ	V <sub>GS</sub> =18V, I <sub>D</sub> =20A	Fig.	
$R_{DS(on)}$	Drain-Source On-State Resistance	/	120	/		V <sub>GS</sub> =18V, I <sub>D</sub> =20A, T <sub>J</sub> =175°C	4,5,6	
			10.4	/	c	V <sub>DS</sub> =20V, I <sub>D</sub> =20A	Fi- 7	
<b>g</b> fs	Transconductance	/	9.2	/	S	V <sub>DS</sub> =20V, I <sub>D</sub> =20A, T <sub>J</sub> =175°C	Fig. 7	
C <sub>iss</sub>	Input Capacitance	/	1200	/		V <sub>GS</sub> =0V	F:_	
C <sub>oss</sub>	Output Capacitance	/	63	/	рF	V <sub>DS</sub> =1000V	Fig.	
C <sub>rss</sub>	Reverse Transfer Capacitance	/	5.7	/		f=1MHz	17,18	
E <sub>oss</sub>	C <sub>oss</sub> Stored Energy	/	41	/	μͿ	V <sub>AC</sub> =25mV	Fig. 16	
E <sub>ON</sub>	Turn-On Switching Energy	/	586	/	1	V <sub>DS</sub> =800V, V <sub>GS</sub> =-4V/18V		
E <sub>OFF</sub>	Turn-Off Switching Energy	/	273	/	μJ	I <sub>D</sub> =20A, R <sub>G(ext)</sub> =2.5Ω, L=100μH		
t <sub>d(on)</sub>	Turn-On Delay Time	/	13	/				
t <sub>r</sub>	Rise Time	/	12	/	]	V <sub>DS</sub> =800V, V <sub>GS</sub> =-4V/18V, I <sub>D</sub> =20A		
t <sub>d(off)</sub>	Turn-Off Delay Time	/	16	/	ns	$R_{G(ext)}=2.5\Omega$ , $R_L=20\Omega$		
t <sub>f</sub>	Fall Time	/	10	/				
R <sub>G(int)</sub>	Internal Gate Resistance	/	5.5	/	Ω	f=1MHz, V <sub>AC</sub> =25mV		
Q <sub>GS</sub>	Gate to Source Charge	/	21.5	/		V <sub>DS</sub> =800V		
$\mathbf{Q}_{GD}$	Gate to Drain Charge	/	14.6	/	nC	V <sub>GS</sub> =-4V/18V	Fig. 12	
$\mathbf{Q}_{G}$	Total Gate Charge	/	68.1	/		I <sub>D</sub> =20A		

#### **Reverse Diode Characteristics**

Symbol	Parameter	Тур.	Max.	Unit	Test Conditions	Note
V	Diode Forward Voltage	4.2	/	V	V <sub>GS</sub> =-4V, I <sub>SD</sub> =10A	Fig.
V <sub>SD</sub>		3.8	/		V <sub>GS</sub> =-4V, I <sub>SD</sub> =10A, T <sub>J</sub> =175°C	8,9,10
Is	Continuous Diode Forward Current	/	33	Α	T <sub>C</sub> =25°C	
t <sub>rr</sub>	Reverse Recover Time	28	/	ns		
Q <sub>rr</sub>	Reverse Recovery Charge	62	/	nC	V <sub>R</sub> =800V, I <sub>SD</sub> =20A	
I <sub>rrm</sub>	Peak Reverse Recovery Current	3.7	/	Α		

#### **Thermal Characteristics**

Symbol	Parameter	Тур.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.84	0.84 / °C/W		Fig. 21	
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient	/	40	C/W		Fig. 21



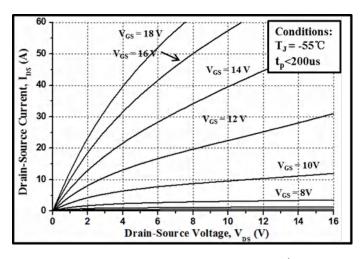


Figure 1. Output Characteristics T<sub>J</sub> = -55°C

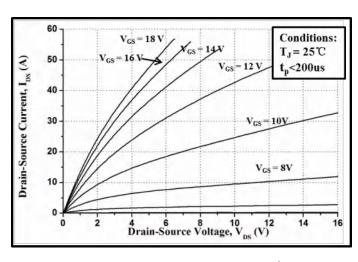


Figure 2. Output Characteristics T<sub>J</sub> = 25°C

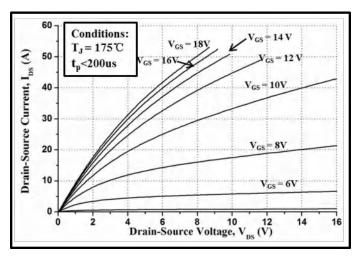


Figure 3. Output Characteristics T<sub>J</sub> = 175°C

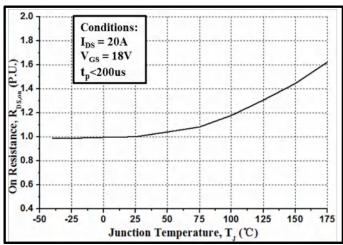


Figure 4. Normalized On-Resistance vs. Temperature

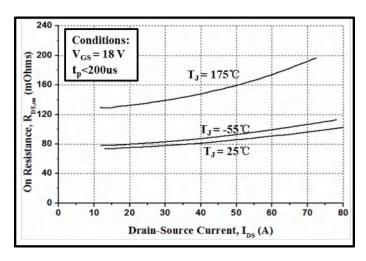


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

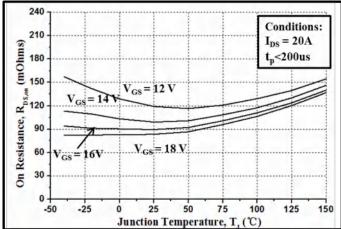


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



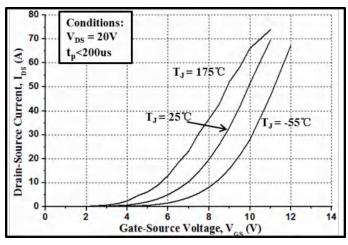


Figure 7. Transfer Characteristic for Various Junction Temperatures

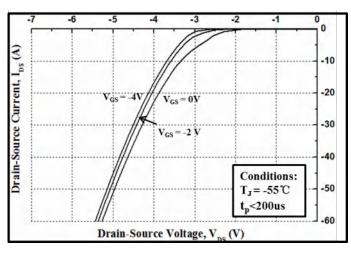


Figure 8. Body Diode Characteristic at -55°C

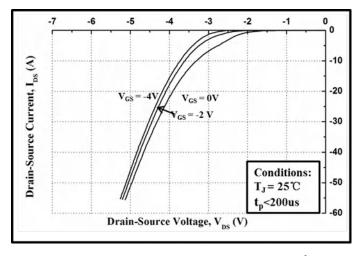


Figure 9. Body Diode Characteristic at 25°C

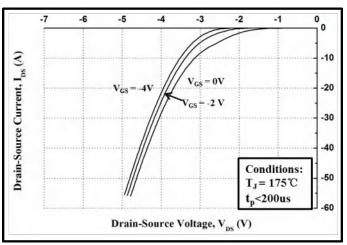


Figure 10. Body Diode Characteristic at 175°C

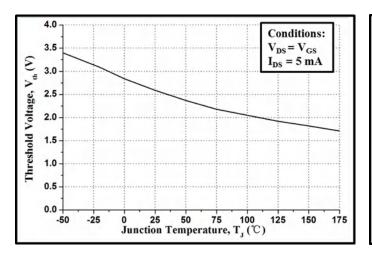


Figure 11. Threshold Voltage vs. Temperature

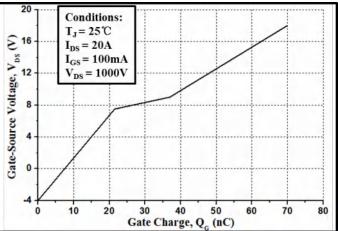
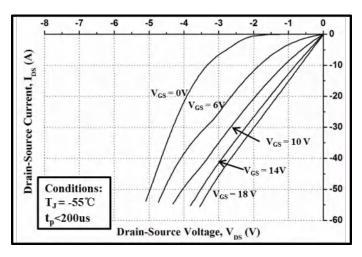


Figure 12. Gate Charge Characteristics

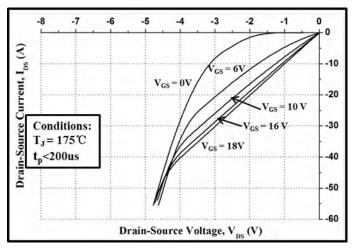




-2 0 20 Drain-Source Current, Ips (A) -40  $V_{GS} = 0V$ -60 -80 -100 -120 -140 -160 Conditions:  $V_{GS} = 18V$ -180 T<sub>J</sub>= 25℃ -200 t<sub>p</sub><200us Drain-Source Voltage, V<sub>DS</sub> (V)

Figure 13. 3rd Quadrant Characteristic at -55°C

Figure 14. 3rd Quadrant Characteristic at 25°C





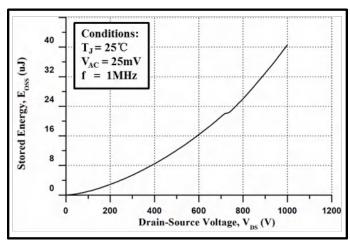


Figure 16. Output Capacitor Stored Energy

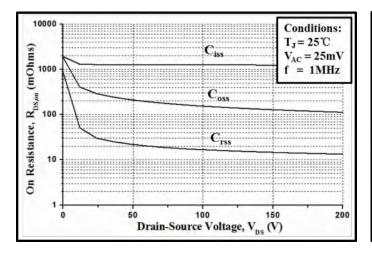


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

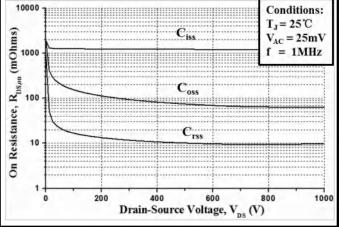
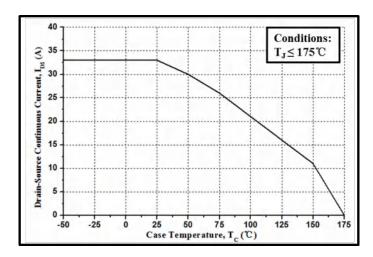


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000V)





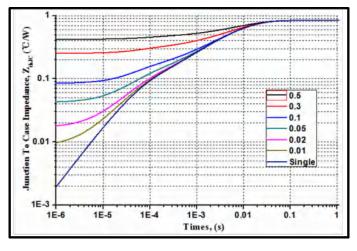
Conditions: 150 (W) 120 (M) T<sub>J</sub>≤175°C Dissip 90 Maximum Power 30 -50 -25 25 50 75 100 125 150 Case Temperature,  $T_c(\mathcal{C})$ 

Figure 19. Continuous Drain Current Derating vs.

Case Temperature

Figure 20. Maximum Power Dissipation Derating vs.

Case Temperature



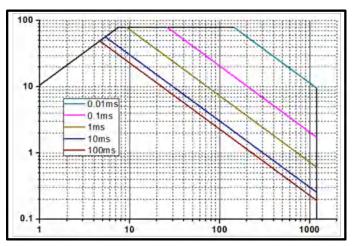


Figure 21. Transient Thermal Impedance (Junction - Case)

Figure 22. Safe Operating Area



#### **Test Circuit Schematic**

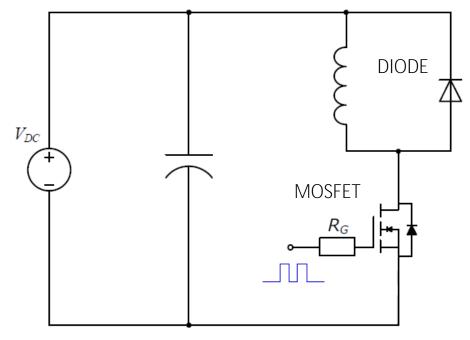
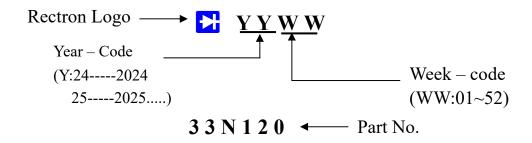


Figure 23. Clamped Inductive Switching
Waveform Test Circuit

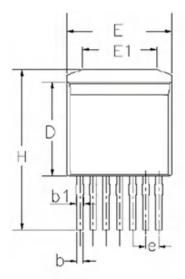


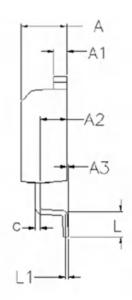
# Marking on the body

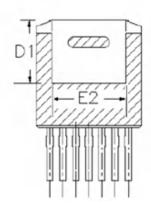


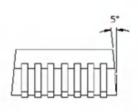


# Package Dimensions









SYMBOLS	DIMENSIONS IN MILLMETERS						
SIMBULS	MIN	NOM	MAX				
A	4.3	4. 43	4.6				
A1	A1 1.2		1.4				
A2	2.4	2.6	2.7				
A3	A3 0		0. 25				
b	0.5	0.6	0.7				
b1	0.6	0.7	0.9				
С	0.4	0.5	0.6				
D	8.88	9. 08	9. 28				
D1	6. 15	6. 45	6.65				
е	1. 27bsc						
E	10.08	10.18	10. 28				
E1	6. 5	7	8.3				
E2	7.3	7.82	7.97				
Н	14.8	15. 5	16				
L	1.9	2.2	2.75				

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